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1 478 810

PATENT SPECIFICATION (11) 1 478 810

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(54) IMPROVEMENTS IN OR RELATING TO DETECTION CIRCUITS FOR MONITORING CURRENT CHANGES

(71) We, STANDARD TELEPHONES AND CABLES LIMITED, a British Company, of 190 Strand, London, W.C.2., England, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electrical circuits for detecting and responding to the change of the current in a circuit being monitored. One example of such a circuit is a telephone subscriber's line in which the condition of the line, unlooped or looped is to be monitored.

In our Application No. 7158/75 (Serial No. 1,478,219) we have described a telephone line monitoring circuit in which the detecting element is a Hall effect device, also known as a Hall relay. Such a device has a magnetic circuit with an air-gap to accommodate the Hall effect element, usually a thin slice of a suitable semiconductor material, there being one or more windings on the magnetic circuit. The current to be monitored flows in the one or more windings, and a control current flows in the Hall effect element. The current flowing in the winding or windings generates a potential difference across the element which is at right-angles to the control current and to the flux due to the current being monitored. This potential difference, and any current flow caused thereby, is proportional both to the magnetic flow and to the control current, and its sense depends on the sense of the field. The output thus produced by the Hall effect element is applied to detection circuitry the output of which is thus indicative of the state of the circuit being monitored.

One of the difficulties encountered with such circuits is the offsets of both the Hall element and the amplifiers which have to be used in the detection circuitry. An object of the present invention is to provide a circuit in which the adverse effects of these offsets is minimised or overcome.

According to the present invention, there is provided an electrical circuit for monitoring the current in an electrical line, which includes a Hall effect device with the energising winding or windings of its magnetic circuit connectable to the line being monitored so that when in use the line current flows in the winding or windings, connections over which when in use a pulsed control current flows across the Hall effect element of the Hall effect device, output connections from said element across which there appears when in use a voltage whose value depends at least on the values of the control current and the line current being monitored, so that the line current is sampled at successive intervals defined by the control current pulses, amplification means to which said voltage is applied and whose output is connected to a storage device, connections from the storage device and the amplification means to comparison means whereby on each sampling of the line current the comparison means compares the value of the instant sample with the value of the preceding sample as stored on the storage device, and means whereby the value of the sample on the storage device is adjusted so that its value corresponds to that of the instant sample, the state of the output from the comparison means reflecting the condition of the line current being monitored.

We have already mentioned that one important application of the invention is to subscribers' line monitoring in telephone systems, which can be either for the detection of calling conditions, or for ring-trip detection. However, it will be clear that the invention is equally applicable to other circuits for monitoring the current flow in an electrical circuit.

Embodiments of the invention will now be described with reference to the accompanying drawings, in which:—

Fig. 1 is a schematic representation of an embodiment of the present invention, with certain waveform used in the circuit shown as an inset.

Fig. 2 is one form that the electronics used in a circuit embodying the invention may

take, again with certain waveforms shown as an inset.

Fig. 3 is a schematic representation of a further embodiment of the invention.

Fig. 4 shows some explanatory waveform.

A first technique in which the invention is exploited compensates for both the Hall element offsets and amplifier offsets. The amplified Hall output voltage is sampled at a suitable rate and stored, e.g. in analogous form on a capacitor, until the next sample. Hence at each sampling time, the current amplified Hall output voltage is compared with the value of that voltage at the preceding sampling time. If there is a difference between the two samples, a change of state in the current in the controlling windings of the Hall device is indicated. As both of these samples include all offset errors, the difference between the two samples is directly proportional only to the difference between the coil current at the two sampling times, the offset errors being automatically eliminated.

The interval between sampling pulses must be greater than the slowest rise-time of the input current waveform, and could be 5—10 ms for use in conjunction with loop disconnect signalling.

A second technique in which the invention is exploited uses the sample and hold technique to compensate for offset effects due to the operational amplifier immediately following the Hall element. This enables the Hall effect device to use a Hall element with a very low output Hall voltage, e.g. as little as the amplifier offset voltage, provided that the Hall element offset is itself low. The principle is based on the fact that when the Hall element is *not* being sampled, the output of the first operational amplifier is a function of its input offsets. The sample is stored on a capacitor for comparison with the voltage output of the first amplifier when the Hall element is being sampled. Here also the difference between the stored voltage and the instant voltage output automatically excludes the input offsets of the first amplifier.

We now turn to Fig. 1, in which the current I_c being monitored is applied to the coil of the Hall effect device, whose element is shown at HE. The biassing current for this element is pulsed, as in the circuits described in the above-mentioned Application, pulses P1 being applied to the base of the transistor T. This pulsing technique provides a useful economy in power consumption. The output from the element HE, which is a voltage whose amplitude and polarity depend on the parameters of I_c, is amplified by an amplifier A. The output of the amplifier A is applied via a switch SW to two comparators VC1 and VC2, and also directly applied to the two comparators.

The switch SW is enabled at the time P3, and its output charges the capacitor C to a level dependent on the magnitude of the sample. Thus the comparators each compare the current value of the sample with the sample's preceding value as stored on C2. From a study of the controlling pulse waveforms it will be seen that this comparison takes place in the first half of the sampling period as defined by P1.

The conditions and connections for the two comparators are such that VC1 has a logic 1 output if $V_s - V_{s-1} \geqslant V_T$, while VC2 has a logic 1 output if $V_{s-1} - V_s \geqslant V_T$. In these relations, V_s is the value of the current sample which is applied directly to the + input of VC1 and the − input of VC2, V_{s-1} is the value of the preceding sample which is applied from C to the − input of VC1 and the + input of VC2, and V_T is less than or equal to half the minimum signal change at the output of A.

The outputs of the two comparators are applied via gates G1 and G2, opened at P2, to a latch 2, which is therefore set to one or other state dependent on whether VC1 or VC2 delivers a 1 output.

Thus the condition of the Hall element is sampled at P1, and the result of this sampling is applied directly to VC1 and VC2 for comparison with the value of the preceding sample. One or other of the comparators therefore has 1 present at its output, and these comparator outputs are effective on the state of the latch L at P2. At time P3, at which pulse P2 has ended, the charge on the capacitor C is adjusted to take account of the condition of the monitored circuit, and this is now ready for use for a comparison to be made with the next sample.

In the circuit of Fig. 2, the output from the Hall effect element is applied to the bases of a long-tailed pair T1—T2 which latter is switched on at pulse S1 which coincides in time with the sampling time of the Hall element. The output of T1—T2, which corresponds to A in Fig. 1, is applied via a sampling gate T3—T4 to a capacitor C1 on which it is stored. The gate T3—T4 is controlled at S2 via further transistors T5—T6 by pulse S2, and corresponds to SW, Fig. 1. Thus it will be seen that the capacitor C1 is charged to a level dependent on the new sample during the second half of S1.

The charge thus present on C1 is applied to the base of transistor T7 and the output of T2 is applied to the base of a further transistor T8, T7 and T8 together forming a long-tailed pair comparator which corresponds functionally to VC1 and VC2 in Fig. 1. The difference voltage thus determined, i.e. the difference between two successive samples is stored in a further capacitor C2. After the sampling and comparison is com-

plete, a further transistor T9 is cut off by the pulse S3, via transistors T10—T11, as is the current in the pair T7—T8, so that the voltage at the collector of T7 rises to the supply voltage level, leaving the voltage at the right-hand end of C2 representing the true Hall effect voltage. This is taken out via an emitter-follower T12 or calibrated with resistors to give a TTL-compatible 1—0 output at the collector of transistor T13.

The sequential timing is indicated from the inset: the new and old samples are compared during the first "half" of the sampling time HC and S1, and the result set into C2 while the new value of the sample is set onto C1 during the second "half" of the sampling time. All current sources to the circuit are via current mirrors for integration purposes. Diode D2 is needed to stop reverse leakage of the charge on C2 via the collector-base diode of T8 when the current is cut off in T7—T8. With a 5 volt power supply an output at the emitter of T12 of 3 to 4 volts is obtainable.

By duplicating the output stage T12—T13 with different thresholds for these transistors a rising or falling edge can be identified. The chip which accommodates the circuitry shown in Fig. 2 can also accommodate a latch, which corresponds to L, Fig. 1, or a Schmidt trigger with adequate noise protection could be used connected to the emitter of T12.

We now turn to Fig. 3, which resembles Fig. 1 in general, except that it uses a single amplifier to perform the functions done by VC1 and VC2 in Fig. 1. In this circuit, R1, R2 and transistor T20 supply the sampling current to the Hall effect element HE under the control of sampling pulses SP applied to R2. The resistor R3, if needed, in series with the element HE limits the maximum sampling current through HE to a safe value. The output voltage of the element HE, which has a value $I_sI_cS_h$, where I_s is the sampling current, I_c the Hall device coil current and S_h the Hall element sensitivity, is applied to the two inputs of an amplifier A10. A10, with the associated resistors R4—R11 form a differential amplifier of gain G with a high common-mode rejection, and it amplifies the Hall voltage and applies it to a switch SW. The resistors R8 and R9 form a potential divider from which a bias voltage V_B for the amplifier A10 is derived.

The switch element SW may use a junction FET, an MOS device, or a bipolar transistor, as in T3—T4 (Fig. 2), and is switched on when the sampling current I_s is off. It charges the sampling capacitor C5 to the output voltage of A10 when the Hall voltage is zero, i.e. to V_B+V_{OFF}, V_{OFF} being the contribution of the offsets of A10 to the output of A10. When the sampling current turns ON, SW is turned off, leaving C5 charged to V_B+V_{OFF}. The sampling current I_s, which flows in R13 in series with the Hall element HE produces a voltage I_sR_s, where R_s is the value of R13, which gives a total voltage of

$$V_B=I_sR_s+V_B+V_{OFF}.$$

The sampling current also generates a Hall voltage giving an output voltage from A10 of

$$V_s=V_B+V_{OFF}+GI_sI_cS_h$$

The amplifier A11 is connected as a comparator for these two voltages so that it has a differential input

$$V_s-V_R=GI_sI_cS_h-I_sR_s$$

which is independent of V_B and V_{OFF}. The value R_s of the current sampling resistor R13 is so chosen that

$$R_s=GS_hI_{CT}$$

where I_{CT} is the desired threshold current in the Hall device coil which to be detected.

Thus the input to the amplifier A11 is

$$GI_sS_h(I_C-I_{CT})$$

the sign of which is independent of I_s, G and S_h and depends only on (I_C-I_{CT}). The logic output from the amplifier A11 is thus low if $I_C>I_{CT}$ and high if $I_C<I_{CT}$.

The capacitor C6 is only used when the circuit is used in a ring trip circuit, in which case it forms, with R14 an integrator to filter out the AC component in the output of A11. The sampling pulse waveforms for loop detection and ring trip detection differ, as will be seen from Fig. 4(a) and (b), which are respectively the waveform used for these functions.

The logic output of A11 is sampled after the sampling current I_s has been turned on but before the charge on C5 has changed significantly, for instance using the technique shown in Fig. 1 with respect to the gates G1, G2.

We have mentioned that a junction FET or an MOS device may be used as the switch SW: in general the latter would be preferred as it is cheaper, and its use would involve a saving in biasing components and therefore also in assembly time.

The sample and hold techniques used in the above circuits compensates for both offset currents and voltages of the first amplifier and also for temperature variations of these. It also compensates for variations, ±5%, of the supply, which variations change the bias voltages and hence the output voltages. Further the circuit also compensates for

sampling current variations in the Hall effect element caused by transistor saturation voltage variations, supply voltage variations (±5%), and variations in the resistance of the Hall element due to manufacturing tolerances and temperature variations (±10%).

It is to be understood that the foregoing description of specific examples of this invention is made by way of example only and is not to be considered as a limitation on its scope.

WHAT WE CLAIM IS:—

1. An electrical circuit for monitoring the current in an electrical line, which includes a Hall effect device with the energising winding or windings of its magnetic circuit connectable to the line being monitored so that when in use the line current flows in the winding or windings, connections over which when in use a pulsed control current flows across the Hall effect element of the Hall effect device, output connections from said element across which there appears when in use a voltage whose value depends at least on the values of the control current and the line current being monitored, so that the line current is sampled at successive intervals defined by the control current pulses, amplification means to which said voltage is applied and whose output is connected to a storage device, connections from the storage device and the amplification means to comparison means whereby on each sampling of the line current the comparison means compares the value of the instant sample with the value of the preceding sample as stored on the storage device, and means whereby the value of the sample on the storage device is adjusted so that the value corresponds to that of the instant sample, the state of the output from the comparison means reflecting the condition of the line current being monitored.

2. An electrical circuit as claimed in claim 1, in which the storage device is a capacitor which is connected via a switch to the output of said amplification means during the second half of the duration of a said sampling, and in which the output of the comparison means is effective during the first half of the duration of the sampling.

3. An electrical circuit as claimed in claim 2, in which the comparison means include a first and a second operational amplifier, in which the capacitor is connected to the negative input of the first operational amplifier and also to the positive input of the second operational amplifier, and in which the amplification means output is connected to the positive input of the first operational amplifier and the negative input of the second operational amplifier, the arrangement being such that the output of one or other of the operational amplifiers is at a logic 1 level dependent on whether the instant sample is larger or smaller than the preceding sample.

4. An electrical circuit as claimed in claim 3, in which said operational amplifiers have their outputs connected respectively via normally-closed gates to the SET and RESET sides of a latch, and in which the gates are opened during the first half of the sampling duration so that the latch can thereby be set to a state dependent on the state of the line being monitored.

5. An electrical circuit as claimed in claim 2, in which the comparison means is a long-tailed transistor pair in which the capacitor is connected to the base of one transistor of the pair while the output of the amplification mean is connected to the base of the other transistor of the pair, in which a further capacitor is connected between the collectors of the two transistors of the pair, which further capacitor is charged to a level dependent on the difference between the instant sample and the immediately preceding sample, and in which the long-tailed pair and said further capacitor are effectively isolated from the rest of the circuit when not actually performing a comparison.

6. An electrical circuit as claimed in claim 2, and in which one end of said capacitor is connected to the output of the amplification means and the other end thereof is connected to a resistor in series with the Hall element so that the value to which the capacitor is set to store a sample takes account amplifier offsets and Hall current variations.

7. An electrical circuit as claimed in claim 6, and in which the comparison means is a single operational amplifier to one input of which the storage capacitor is connected and to the other input of which the output of the amplification means is connected.

8. An electrical circuit for monitoring the current flowing in an electrical line substantially as described with reference to Fig. 1, Fig. 2 or Fig. 3 of the accompanying drawings.

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For the Applicants.

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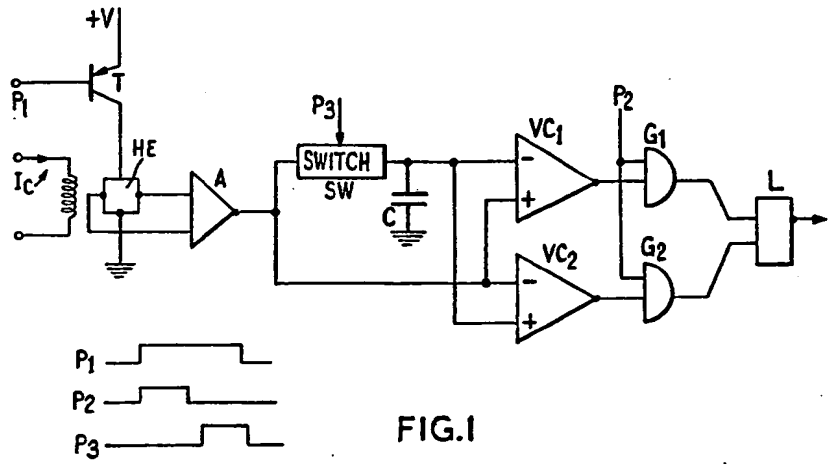

FIG.1

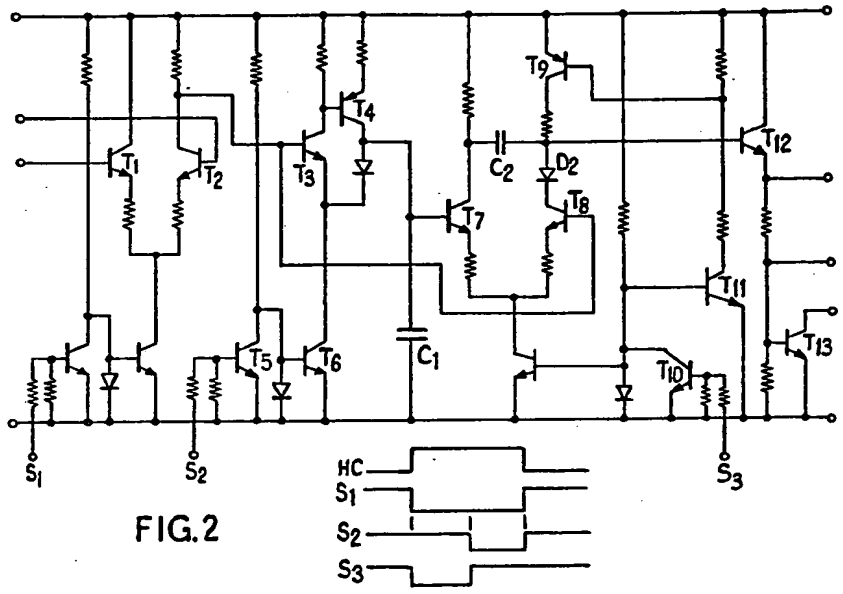

FIG.2

1478810 COMPLETE SPECIFICATION
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Sheet 2

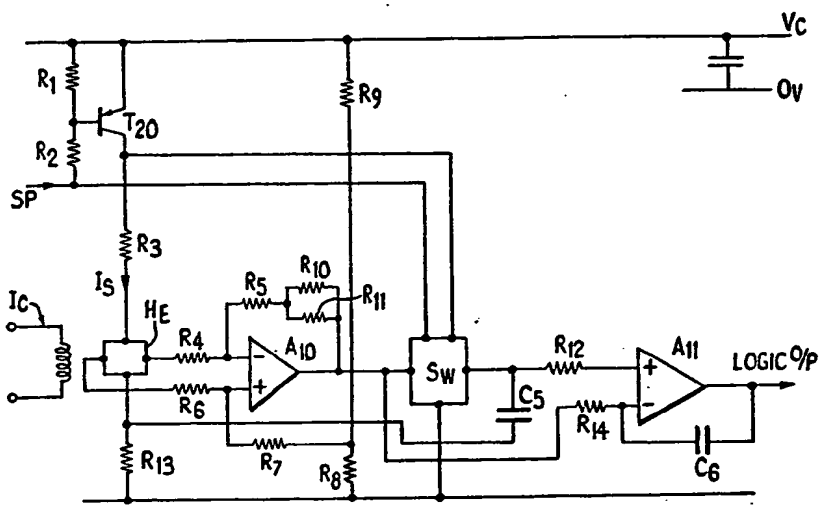

FIG.3

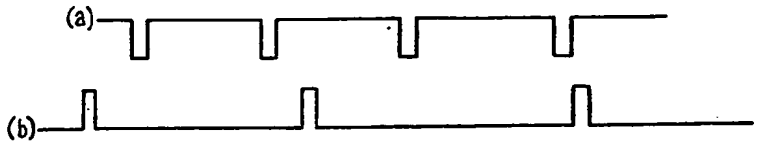

FIG.4